a baseband signal processing network for receiving said baseband signal streams and providing cross-correlated and filtered Bit Rate Agile (BRA) in-phase and quadrature-phase baseband signals;

a Quadrature Modulator serving to quadrature modulate said cross-correlated filtered in-phase and quadrature-phase baseband signals;

an interface transmitter port to provide said quadrature modulated signal to the transmission medium;

an interface receiver port to provide connection of the said cross-correlated filtered quadrature modulated signal to the demodulator; and

a demodulator structure to serve for Bit Rate Agile (BRA) signal demodulation having Bit Rate Agile (BRA) demodulation filters Mis-Matched (MM) to that of the modulator filters.

2. (Amended) The structure as in Claim 1 wherein said processed in-phase and quadrature-phase baseband signals have amplitudes such that their vector sum is substantially constant and has reduced resultant quadrature modulated envelope fluctuations.

4. (Amended) A cross-correlated signal processor for Bit Rate Agile (BRA), Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) wireless systems including bit rate agile wireless CDMA, GSM, OFDM and TDMA systems, the signal processor comprising:

(a) means for providing in-phase and quadrature-phase signals;

(b) means for cross-correlating a fraction of a symbol or one or more than one symbol of the in-phase (I) signal with a fraction of a symbol or one or more than one symbol of the quadrature-phase (Q) signal;

(c) means for generating filtered cross-correlated I and Q signals;

(d) means for implementing the cross-correlated signals by analog active or passive circuits, by digital circuits or combination thereof;

(e) means for providing a control circuit to select from a set of predetermined cross-correlated waveforms provided to filters in the I and/or Q channels;

(f) means for Quadrature modulating the I and Q signals;

(g) means for Linear and/or Nonlinear amplification to provide to the antenna;

(h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator;

(i) a BRA and MFS quadrature demodulator; and

(j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the said demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

5. (Amended) Cross-correlated signal processor means for Bit Rate Agile (BRA) and Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) means comprising:

(a) processing means for one or more input signals and providing in-phase (I) and quadrature-phase shifted (Q) signals;

(b) means for cross-correlating the in-phase and quadrature shifted signals;

(c) means for generating in-phase and quadrature-phase shifted output signals having amplitudes such that the vector sum of the output signals is approximately the same at virtually all phase angles of each bit period for one set of cross-correlation and filter parameters and the vector sum is not constant for an other set of chosen filter parameters;

(d) means for quadrature modulating the in-phase and quadrature output signals, to provide a cross-correlated modulated output signal;

(e) means for providing a control circuit to select from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels;

(f) means for Quadrature modulating the I and Q signals;

(g) means for Linear and/or Nonlinear amplification to provide to the antenna

(h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator;

(i) a BRA and MFS quadrature demodulator; and

(j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

6. (Amended) A cross-correlated signal processor comprising:

(a) means for cross-correlating a fraction, or one or more than one symbol synchronous and/or asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a

quadrature-phase shifted signal of the in-phase signal, and providing in-phase (I) and quadrature-phase (Q) shifted signals for Bit Rate Agile (BRA), cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, according to the following schedule:

(i) when the in-phase channel signal is zero, the quadrature shifted signal is close to the maximum amplitude normalized to one (1);

(ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature shifted signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

(iii) when the quadrature channel signal is zero, the in-phase signal close to the maximum amplitude;

(iv) when the quadrature channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

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(b) means for quadrature modulating the in-phase and quadrature output signals to provide a cross-correlated modulated output signal;

(c) controlling means and signal selection means for BRA rate, MFS and CS processor selection and selection for Linear and/or Non-Linearly Amplified (NLA) baseband and/or of Quadrature modulated signals;

(d) coupling port means to the transmission medium;

(e) a receiver port for connection of the received cross-correlated signal to the BRA, MFS and CS demodulator;

(f) a BRA, MFS and CS quadrature demodulator; and

(g) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which the said demodulator filter set is MM to that of the BRA, MFS and BRA filter set of the modulator.

Cancel Claims 8-9 without prejudice in response to restriction/election requirement.

8. (Cancelled) An adaptive equalizer structure comprising:

an interface receiver port to provide connection of received modulated signal to the pre-demodulation adaptive equalizer;

a pre-demodulation adaptive equalizer structure comprising splitter, multiplier and delay structure for generating a control signal and received modulated signal time delayed product in one branch of the splitter and coupling the signal time delayed product in one branch of the

splitter and the said received modulating signal in the other branch of the splitter to a signal combiner;

a signal combiner structure for combining the said delayed control signal and received modulated signal product;

a demodulator structure for demodulating the combined delayed control signal and received modulated signal product; and

a control signal processor for generation of and connection of said control signal to the said product multiplier circuit.

9. (Cancelled) An adaptive equalizer and switchable delay structure comprising:

an interface receiver port to provide connection of received modulated signal to a plurality of splitters, amplifiers, delay elements and signal combiners for signal selection of said received modulated signal;

a demodulator structure for demodulating the selected received modulated signal; and

a control signal processor for generation of said control signal.

Add Claims 10-58 as follows:

10. (New) The structure as in claim 2, further comprising means for selectively reducing the cross-correlating factor down to zero.

11. (New) A cross-correlated signal processor for Bit Rate Agile (BRA) wireless systems and signal environments including bit rate agile wireless CDMA, GSM, OFDM and TDMA systems and signal environments, the signal processor comprising:

(a) an input adapted to receive in-phase (I) and quadrature-phase (Q) signals;

(b) a cross-correlator for cross-correlating a fraction of a symbol or one or more than one symbol of the in-phase (I) signal with a fraction of a symbol or one or more than one symbol of the quadrature-phase (Q) signal;

(c) a circuit generating the cross-correlated signals; and

(d) a control circuit selecting particular cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels.

12. (New) The cross-correlated signal processor in claim 11, further comprising:

(e) a quadrature modulator for quadrature modulating the I and Q signals.

13. (New) The cross-correlated signal processor in claim 12, further comprising:

(f) an amplifier for amplifying the quadrature modulated signals.

14. (New) The cross-correlated signal processor in claim 13, wherein the amplifier comprises a linear amplifier operating in a substantially linear amplification range and providing substantially linear amplification.

15. (New) The cross-correlated signal processor in claim 13, wherein the amplifier comprises a non-linear amplifier operating in at least a partially non-linear amplification range and providing at least a partial of non-linear amplification.

16. (New) The cross-correlated signal processor in claim 13, wherein the amplifier comprises a linear amplifier stage and a non-linear amplifier stage.

17. (New) The cross-correlated signal processor in claim 13, wherein the amplifier is coupled or couplable to an external transmit antenna and provides amplified signals to the antenna, the external transmit antenna for transmitting the cross-correlated amplified signals.

18. (New) The cross-correlated signal processor in claim 13, wherein the cross-correlated processor further comprises (h) the external transmit antenna for transmitting the cross-correlated amplified signals.

19. (New) The cross-correlated signal processor in claim 17, wherein the transmitted cross-correlated amplified signals are adapted to be received by an external receive antenna.

20. (New) The cross-correlated signal processor in claim 18, wherein the transmitted cross-correlated amplified signals are adapted to be received by an external receive antenna.

21. (New) The cross-correlated signal processor in claim 17, further comprising:

(i) the external receive antenna for receiving the transmitted cross-correlated amplified signals.

22. (New) The cross-correlated signal processor in claim 18, further comprising:

(i) the external receive antenna for receiving the transmitted cross-correlated amplified signals.

23. (New) The cross-correlated signal processor in claim 19, further comprising:

(j) a receiver port for receiving a received modulated cross-correlated amplified signal from the receive antenna; and

(k) a quadrature demodulator coupled for communication with the receiver port and receiving the received modulated cross-correlated amplified signal .

24. (New) The cross-correlated signal processor in claim 23, wherein the quadrature demodulator comprises a BRA and MFS signal capable quadrature demodulator.

25. (New) The cross-correlated signal processor in claim 24, further comprising:

(l) a mis-matched (MM) BRA and MFS demodulator filter set.

26. (New) The cross-correlated signal processor in claim 12, wherein the quadrature modulator includes a first BRA and MFS filter set.

27. (New) The cross-correlated signal processor in claim 24, wherein the quadrature demodulator includes a second BRA and MFS filter set.

28. (New) The cross-correlated signal processor in claim 24, wherein:

the quadrature modulator includes a first BRA and MFS filter set;

the quadrature demodulator includes a second BRA and MFS filter set; and

the quadrature demodulator second BRA and MFS filter set is mis-matched to the quadrature modulator first BRA and MFS filter set.

29. (New) The cross-correlated signal processor in claim 24, wherein the demodulator includes a filter set that is mis-matched to that of the BRA and MFS filter set of the modulator.

30. (New) The cross-correlated signal processor in claim 25, wherein the demodulator filter set is mis-matched to that of the BRA and MFS filter set of the modulator.

31. (New) The cross-correlated signal processor in claim 28, wherein the circuit generating the cross-correlated signals comprises a circuit selected from the set of circuit types consisting of an one or a plurality of analog active circuits, one or a plurality of analog passive circuits, one or a plurality of digital circuits, and combinations thereof.

32. (New) The cross-correlated signal processor in claim 11, wherein the circuit generating the cross-correlated signals comprises a circuit selected from the set of circuit types consisting of an one or a plurality of analog active circuits, one or a plurality of analog passive circuits, one or a plurality of digital circuits, and combinations thereof.

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33. (New) The cross-correlated signal processor in claim 22, wherein a single antenna serves as the receive antenna and the transmit antenna.

34. (New) A signal processor comprising:

an input circuit providing in-phase (I) and quadrature-phase (Q) shifted signals;

a cross-correlator for cross-correlating the in-phase and quadrature-phase shifted signals;

a signal generator for generating in-phase and quadrature-phase shifted output signals having amplitudes such that the vector sum of the output signals is substantially the same at virtually all phase angles of each bit period for one set of cross-correlation and filter parameters and the vector sum is not substantially the same for another set of chosen filter parameters;

a control circuit for selecting particular cross-correlated signal elements filters and waveforms in the I and/or Q channels from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels; and

a quadrature modulator for quadrature modulating the I and Q signals to generate a cross-correlated modulated output signal.

35. (New) The signal processor in claim 34, further comprising:

an amplifier performing linear and/or non-linear amplification of the quadrature modulated I and Q signals, the amplified signals coupled to an external transmit antenna for transmission of a transmit signal, the transmit signal being an amplified quadrature modulated cross-correlated signal.

36. (New) The signal processor in claim 35, further comprising:

a receiver port coupled to an external receive antenna for receiving the transmitted amplified quadrature modulated cross-correlated signal for connection to an external BRA and MFS quadrature demodulator.

37. (New) The signal processor in claim 36, further comprising the external BRA and MFS quadrature demodulator.

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38. (New) The signal processor in claim 36, further comprising the external receive antenna.

39. (New) The signal processor in claim 37, wherein the quadrature modulator includes a BRA and MFS filter set.

40. (New) The signal processor in claim 39, further comprising:

a Mis-Matched (MM) BRA and MFS demodulator filter set.

41. (New) The signal processor in claim 40, wherein the demodulator filter set is mis-matched to that of the BRA and MFS filter set of the modulator.

42. (New) The signal processor in claim 34, wherein the input circuit includes signal processing circuitry for processing one or more input signals to generate in-phase (I) and quadrature-phase (Q) shifted signals from the one or more input signals.

43. (New) A cross-correlated signal processor comprising:

(a) a cross-correlator for cross-correlating a fraction, or one or more than one symbol synchronous and/or asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a quadrature-phase shifted signal of the in-phase signal, and providing in-phase (I) and quadrature-phase (Q) shifted signals for Bit Rate Agile (BRA), cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, according to the following schedule:

(i) when the in-phase channel signal is zero, the quadrature shifted signal is close to the maximum amplitude normalized to one (1);

(ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature shifted signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

(iii) when the quadrature channel signal is zero, the in-phase signal close to the maximum amplitude;

(iv) when the quadrature channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

(b) a signal modulator for quadrature modulating the in-phase and quadrature output signals to provide a cross-correlated modulated output signal;

(c) a controller and selector for selecting at least one of or any combination of: BRA rate, MFS and CS processor selection, and selection for Linear and/or Non-Linearly Amplified (NLA) baseband and/or of quadrature modulated signals;

(d) a first signal coupling for coupling a cross-correlated output signal to a transmission medium;

(e) a second signal coupling for coupling a received cross-correlated signal from the transmission medium to a receiver port;

(f) a receiver port for connection of the received cross-correlated signal to the BRA, MFS and CS demodulator;

(g) a BRA, MFS and CS quadrature demodulator; and

(h) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which the said demodulator filter set is MM to that of the BRA, MFS and BRA filter set of the modulator.

44. (New) A method of processing signals for Bit Rate Agile (BRA) and Modulation-Demodulation Format Selectable (MFS) and Code Selectable (CS) signal environments, the method comprising:

receiving in-phase (I) and quadrature-phase (Q) signals;

cross-correlating a fraction of a symbol or one or more than one symbol of the in-phase (I) signal with a fraction of a symbol or one or more than one symbol of the quadrature-phase (Q) signal;

filtering the cross-correlated I and Q signals to generate filtered cross-correlated I and Q signals; and

selecting particular cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels.

45. (New) The method in claim 44, further comprising: modulating the I and Q signals to generate quadrature modulated cross-correlated signals.

46. (New) The method in claim 45, further comprising: amplifying the quadrature modulated signals.

47. (New) The method in claim 46, wherein the amplification providing substantially linear amplification.

48. (New) The method in claim 46, wherein the amplification providing at least a portion of non-linear amplification (NLA).

49. (New) The method in claim 46, wherein the amplification providing a portion of linear amplification and at least a portion of non-linear amplification (NLA).

50. (New) The method in claim 46, wherein the amplifier is coupled or couplable to an external transmit antenna and the method further comprising transmitting the quadrature modulated cross-correlated amplified signals to a transmission medium.

51. (New) The method in claim 50, further comprising receiving the transmitted quadrature modulated cross-correlated amplified signal from the transmission medium.

52. (New) The method in claim 51, further comprising demodulating the received or communication with the receiver port and receiving the received quadrature modulated cross-correlated amplified signal .

53. (New) The method in claim 52, wherein the quadrature demodulating comprises at least one of BRA and MFS quadrature demodulation.

54. (New) The method in claim 53, wherein the quadrature modulation includes modulating with a first BRA and MFS filter set.

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55. (New) The method in claim 54, wherein the quadrature demodulator includes a second BRA and MFS filter set.

56. (New) The method in claim 53, wherein:

the quadrature modulation includes a first BRA and MFS filter set;

the quadrature demodulation includes a second BRA and MFS filter set; and

the quadrature demodulation second BRA and MFS filter set is different from the quadrature modulation first BRA and MFS filter set.

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57. (New) The cross-correlated signal processor of Claim 43, wherein the cross-correlated signal processor is adapted to process (i) a first in-phase channel signal set component; and (ii) a second quadrature-phase channel signal set component that is generated as a phase-shifted version of the first in-phase channel signal;

the in-phase and quadrature-phase channel signals characterized in that: (i) when the in-phase channel signal is zero, the quadrature-phase shifted signal is close to the maximum amplitude normalized to one (1); (ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature-phase shifted signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$; (iii) when the quadrature-phase channel signal is zero, the in-phase signal close to the

maximum amplitude; and (iv) when the quadrature-phase channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$; and

the first in-phase and second quadrature-phase signal set components derived from at least one signal stream as a fraction a symbol or from one or more than one symbol as a time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a quadrature-phase shifted signal of the in-phase signal.

58. (New) A bit-rate agile (BRA) and modem format and code selectable (MFS and CS) signal pair comprising:

a first in-phase channel signal set component; and

a second quadrature-phase channel signal set component that is generated as a phase-shifted version of the first in-phase channel signal;

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the in-phase and quadrature-phase channel signals characterized in that: (i) when the in-phase channel signal is zero, the quadrature-phase shifted signal is close to the maximum amplitude normalized to one (1); (ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature-phase shifted signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$; (iii) when the quadrature-phase channel signal is zero, the in-phase signal close to the maximum amplitude; and (iv) when the quadrature-phase channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$; and

the first in-phase and second quadrature-phase signal set components derived from at least one signal stream as a fraction a symbol or from one or more than one symbol as a time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a quadrature-phase shifted signal of the in-phase signal.